UNIT–V
ADVANCED ARM PROCESSORS

S.No		Questions	BT	CO	PO
Part – A (Short Answer Questions)					
1		Illustrate different Registers and Special Registers in Cortex M3 processor	L2	Co5	PO1, PO2
2		Briefly describe the features of the Cortex M3 based microcontrollers memory organization.	L3	Co5	PO1, PO2
3		Write about Bus Interfaces in ARM Cortex M3 processor.	L3	Co5	PO1, PO2
4		What are the major address ranges in Memory Map of Cortex M3	L3	Co5	PO1, PO2
5		What is Pipeline mechanism? Explain briefly the pipeline mechanism in Cortex-M3 Processor.	L3	Co5	PO1, PO2
6		Introduce a GPIO pin handling with a Cortex M core controller	L4	Co5	PO1, PO2
7		Introduce the typical energy-saving modes of 8-bit and 32-bit microcontrollers	L2	Co5	PO1, PO2
8		Briefly compare the properties of Cortex M0, M3, M4, M7 cores	L3	Co5	PO1, PO2
9		Discuss the features of OMAP processor	L2	Co5	PO1, PO2
10		Explain about combined program status register	L2	Co5	PO1, PO2
Part – B (Long Answer Questions)					
11	a)	What are the features of arm cortex processor	L1	Co5	PO1, PO2
	b)	Expalin about memory mapping of cortex processor	L2	Co5	PO1, PO2
12	a)	List out all general purpose registers and Special purpose Registers with application	L2	Co5	PO1, PO2
	b)	Discuss Combined program status Register and expalin each flag	L2	Co5	PO1, PO2
13	a)	Draw and explain "Thumb programmer's model	L2	Co5	PO1, PO2
	b)	Differentiate between ARM processor and OMAP processor	L2	Co5	PO1, PO2
14	a)	Briefly describe the features of the Cortex M3 based microcontrollers memory organization. What are the major address ranges? What is bit banding, what is nonaligned memory access. What are the main differences comparing to	L4	Co5	PO1, PO2

		ARM7-based controllers?			
	b)	Describe a typical clock tree of a Cortex M core microcontroller. Explain the meaning and necessity of each clock signal source as well as clock signal divisions.	L4	Co5	PO1, PO2
15	a)	Briefly describe the features of the Cortex M3 based microcontrollers memory organization.	L4	Co5	PO1, PO2
	b)	What is Pipeline mechanism? Explain briefly the pipeline mechanism in Cortex-M3 Processor.	L2	Co5	PO1, PO2
16	a)	Differentiate between CORTEX processor and OMAP processor	L4	Co5	PO1, PO2
	b)	Discuss the features of OMAP processor	L2	Co5	PO1, PO2

* **Blooms Taxonomy Level (BT)** (L1 – Remembering; L2 – Understanding; L3 – Applying; L4 – Analyzing; L5 – Evaluating; L6 –Creating)

Course Outcomes (CO)

Program Outcomes(PO)

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